REMARKS

Claims 1-23 are pending in the present application. Claims 1, 9, 17, and 21 are amended above. New claims 24 and 25 are added above. No new matter is added by the claim amendments or new claims. Entry is respectfully requested.

The applicants note, with appreciation, that the Office Action indicates at page 3, paragraph 1, that independent claim 23 is allowed. It is further noted that the Office Action indicates at page 2, paragraph 3, that claims 2-4, 10-12, and 18-20 would be allowable if rewritten in independent form. Accordingly, new claim 24 is added to incorporate the limitations of claim 4. New claim 25 is added to incorporate the limitations of claim 12. With regard to claims 2, 3, 10, 11, and 18-20, the applicants wish to defer submission of these claims, pending consideration of the present amendment. Entry and allowance of the claims are respectfully requested.

Claim 1, 5-9, 13-17, and 21 stands rejected under 35 U.S.C. 102(b) as being anticipated by Wada, *et al.* (U.S. Patent No. 5,886,388). Reconsideration of the rejection and allowance the claims are respectfully requested.

The present invention as claimed in independent claim 1 is directed to an SRAM. The SRAM includes a first and a second access NMOS transistor. The SRAM further includes a first inverter comprising a first drive NMOS transistor and a first load PMOS transistor. The first inverter is selectively activated in response to the operation of the second access NMOS transistor. The SRAM further includes a second inverter that includes a second drive NMOS

transistor and a second load PMOS transistor. The second inverter is selectively activated in response to the operation of the first access NMOS transistor. The transistors are formed on active areas of an SOI substrate. A portion of an active area where a load PMOS transistor is formed extends so as to make a predetermined acute angle with a portion of an active area where a drive NMOS transistor is formed.

The present invention as claimed in independent claim 9 is directed to an SRAM. The SRAM includes a semiconductor substrate. The SRAM further includes a first active area formed on the semiconductor substrate. The first active area includes a first access NMOS transistor and a first inverter which includes a first drive NMOS transistor and a first load PMOS transistor. The SRAM further includes a second active area formed on the semiconductor substrate. The second active area includes a second access NMOS transistor and a second inverter which includes a second drive NMOS transistor and a second load PMOS transistor. A portion of each of the first and second active areas where the first and second load PMOS transistors are formed, respectively, extends so as to make a predetermined acute angle with a portion of each of the first and second active areas where the NMOS transistors are formed.

The present invention as claimed in independent claim 17 is directed to an SRAM. The SRAM is formed with first and second access NMOS transistors, and a first inverter that includes a first drive NMOS transistor and a first load PMOS transistor. The first inverter is selectively activated in response to the operation of the second access NMOS transistor. The SRAM further includes a second inverter that includes a second drive NMOS transistor and a second load PMOS transistor. The second inverter is selectively activated in response to the operation of the

first access NMOS transistor. The SRAM includes an SOI substrate. The SRAM further includes a first active area on the SOI substrate. The first active area includes a first access NMOS transistor and a first inverter which includes a first drive NMOS transistor and a first load PMOS transistor. The SRAM further includes a second active area formed on the SOI substrate. The second active area includes a second access NMOS transistor and a second inverter which includes a second drive NMOS transistor and a second load PMOS transistor. A portion of each of the first and second active areas where the first and second load PMOS transistors are formed, respectively, extends so as to make a predetermined acute angle with a portion of each of the first and second active areas where the NMOS transistors are formed.

The present invention as claimed in independent claim 21 is directed to an SRAM. The SRAM is formed with first and second access NMOS transistors, and a first inverter that includes a first drive NMOS transistor and a first load PMOS transistor. The first inverter is selectively activated in response to the operation of the second access NMOS transistor. The SRAM is further formed of a second inverter that includes a second drive NMOS transistor and a second load PMOS transistor. The second inverter is selectively activated in response to the operation of the first access NMOS transistor. The SRAM includes an SOI substrate. The SRAM includes a first active area on the SOI substrate. The first active area includes a first access NMOS transistor and a first inverter which includes a first drive NMOS transistor and a first load PMOS transistor. The SRAM further includes a second active area formed on the SOI substrate. The second active area includes a second access NMOS transistor and a second inverter which includes a second drive NMOS transistor and a second load PMOS transistor. A portion of each of the first and second active areas where the first and second load PMOS transistors are formed,

respectively, extend so as to make a predetermined acute angle with a portion of each of the first and second active areas where the NMOS transistors are formed. One of the drain and source of the first access NMOS transistor, the drain of the first drive NMOS transistor, and the drain of the first load PMOS transistor are formed in a shared region of the first active area so as to be electrically connected to one another. One of the drain and source of the second access NMOS transistor, the drain of the second drive NMOS transistor, and the drain of the second load PMOS transistor are formed in a shared region of the second active area so as to be electrically connected to one another.

In the present invention as claimed in independent claim 1, an SRAM includes "a portion of an active area where a load PMOS transistor is formed" that extends "so as to make a predetermined acute angle with a portion of an active area where a drive NMOS transistor is formed"(emphasis added). In the present invention as claimed in independent claims 9, 17, and 21, an SRAM includes "a portion of each of the first and second active areas where the first and second load PMOS transistors are formed" that extends "so as to make a predetermined acute angle with a portion of each of the first and second active areas where the NMOS transistors are formed"(emphasis added). By orienting the active areas where the PMOS transistors are formed at a "predetermined acute angle" with the active areas where the NMOS transistors are formed, the effective hole mobility of the PMOS transistors is increased (see Specification, page 8, lines 8-16).

Wada discloses a static semiconductor memory device including a PMOS transistor active area that makes a 90 degree angle with the NMOS transistor active area. Therefore, Wada

fails to teach or suggest "a portion of an active area where a load PMOS transistor is formed" extending "so as to make a predetermined acute angle with a portion of an active area where a drive NMOS transistor is formed", as claimed in independent claim 1, or "a portion of each of the first and second active areas where the first and second load PMOS transistors are formed" extending "so as to make a predetermined acute angle with a portion of each of the first and second active areas where the NMOS transistors are formed", as claimed in independent claims 9, 17, and 21. The 90-degree orientation of Wada is not acute and would therefore not take advantage of increased effective hole mobility. Reconsideration and removal of the rejection of claims 1, 9, 17, and 21 under 35 U.S.C. 102(b) as being anticipated by Wada are respectfully requested.

It is therefore submitted that independent claims 1, 9, 17, and 21 are in condition for allowance, and such allowance is respectfully requested. With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.